What is Claimed is:

1. Logic module circuitry comprising:

combinational logic circuitry having at least first, second, and third stages; and

XOR circuitry interposed between two of the stages or between the third stage and an output of the combinational logic circuitry for logically combining a carry in signal with at least one combinational signal in the combinational logic circuitry.

2. The circuitry defined in claim 1 further comprising:

programmably controlled circuitry for selectively disabling the carry in signal.

3. The circuitry defined in claim 1 further comprising:

circuitry for producing a carry out signal from the carry in signal and combinational signals in the combinational logic circuitry.

4. The circuitry defined in claim 3 wherein the circuitry for producing comprises:

multiplexer circuitry for using a first of the combinational signals to control selection of one of the carry in signal and a second of the combinational signals as the carry out signal.

5. The circuitry defined in claim 4 wherein the multiplexer circuitry comprises:

a first path for selectively conveying, at a relatively high speed, signal information

indicative of the carry in signal to a lead for signal information indicative of the carry out signal; and

a second path for selectively conveying, at less than the relatively high speed, signal information indicative of the second of the combinational signals to the lead for signal information indicative of the carry out signal.

6. The circuitry defined in claim 5 wherein the first path comprises:

an inverter with a virtual power supply and ground enabled by the first of the combinational signals.

7. The circuitry defined in claim 6 wherein the second path comprises:

an inverter and CMOS pass gate.

8. The circuitry defined in claim 1 wherein the combinational logic circuitry has first, second, third, and fourth stages, and wherein the XOR circuitry is interposed between the third and fourth stages.

9. The circuitry defined in claim 1 wherein the XOR circuitry is interposed between the second and third stages.

10. The circuitry defined in claim 1 wherein the third stage has first and second combinational signal outputs, and wherein the XOR circuitry logically combines the first combinational signal output with the carry in signal to produce a sum out signal.

11. The circuitry defined in claim 10 further comprising:

circuitry for producing a carry out signal from the carry in signal and the first and second combinational signal outputs.

12. The circuitry defined in claim 11 wherein the circuitry for producing comprises circuitry for using the first combinational signal output to select one of the carry in signal and the second combinational signal output as the carry out signal.

13. The circuitry defined in claim 1 wherein the second stage has first, second, third, and fourth combinational signal outputs, and wherein the XOR circuitry logically combines the carry in signal with each of the first and second combinational signal outputs to produce two further signals for application to the third stage.

14. The circuitry defined in claim 13 further comprising:

circuitry for producing a carry out signal from the carry in signal, the first and second combinational signal outputs, a third stage combinational signal output based on the third and fourth combinational signal outputs, and a third stage input signal.

15. The circuitry defined in claim 14 wherein the circuitry for producing comprises:

circuitry for using the third stage input signal to select one of the first and second combinational signal outputs as a control signal; and

circuitry for using the control signal to select one of the carry in signal and the third

stage combinational signal output as the carry out signal.

16. The circuitry defined in claim 1 wherein the first and second stages are programmable to produce an output signal that is usable in forming an arithmetic sum of first and second stage input signals.

17. The circuitry defined in claim 1 wherein the first and second stages are programmable to produce an output signal that is usable in forming an arithmetic difference between first and second stage input signals.

18. The circuitry defined in claim 1 wherein the first and second stages are programmable to produce an output signal that is usable in forming an arithmetic product of first and second stage input signals.

19. The circuitry defined in claim 18 wherein the third stage and the XOR circuitry are operable to form the arithmetic sum of the output signal, a third stage input signal, and a carry in signal.

20. A programmable logic device comprising logic module circuitry as defined in claim 1.

21. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

a programmable logic device as defined in claim 20 coupled to the processing circuitry and the memory.

22. A printed circuit board on which is mounted a programmable logic device as defined in claim 20.

23. The printed circuit board defined in claim 22 further comprising:

a memory mounted on the printed circuit board and coupled to the programmable logic device.

24. The printed circuit board defined in claim 22 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the programmable logic device.

25. The method of operating combinational logic that includes at least first, second, and third stages comprising:

using XOR circuitry that is connected between two of the stages or between the third stage and an output of the combinational logic circuitry to logically combine a carry in signal with at least one combinational signal produced by the combinational logic.

26. The method defined in claim 25 further comprising:

programming the first and second stages so that they can produce an output signal that is usable in forming an arithmetic sum of first and second stage input signals.

27. The method defined in claim 26 wherein the using comprises:

employing the XOR circuitry to produce a further arithmetic sum of the output signal and the carry in signal.

28. The method defined in claim 27 further comprising:

additionally programming the first and second stages so that they can produce signals for use in providing a carry out signal that results from an arithmetic summation of the first and second stage input signals and the carry in signal.

29. The method defined in claim 25 further comprising:

programming the first and second stages so that they can produce an output signal that is usable in forming an arithmetic product of first and second stage input signals.

30. The method defined in claim 29 further comprising:

using the third stage and the XOR circuitry to form an arithmetic sum of the output signal, the carry in signal, and a third stage input signal.

31. The method defined in claim 30 further comprising:

additionally programming the first and second stages so that they can produce signals for use in providing a carry out signal that results from an

arithmetic summation of the output signal, the carry in signal, and the third stage input signal.

32. Logic module circuitry comprising:

look-up table circuitry having first, second, third, and fourth stages; and

XOR circuitry connected between two of the stages that are selected from the group consisting of (1) the second and third stages, and (2) the third and fourth stages, the first-mentioned stage in the selected group being a source stage, and the second-mentioned stage in the selected group being a destination stage, the XOR circuitry logically combining a carry in signal with signal information from the source stage to produce further signal information applied to the destination stage.

33. The circuitry defined in claim 32 further comprising:

circuitry for selectively disabling the carry in signal.

34. The circuitry defined in claim 32 further comprising:

circuitry for producing a carry out signal from at least the carry in signal and signal information from the source stage.

35. The circuitry defined in claim 34 wherein the circuitry for producing is connected so that the carry out signal is based in part on a third stage input signal.

36. The circuitry defined in claim 32 wherein the look-up table circuit leading to the XOR

circuitry includes circuit elements that are programmable so that the signal information from the source stage that the XOR circuitry receives is indicative of a result of arithmetically adding together first and second stage input signals.

37. The circuitry defined in claim 32 wherein the look-up table circuitry leading to the XOR circuitry includes circuit elements that are programmable so that the signal information from the source stage that the XOR circuitry receives is based at least in part on a result of arithmetically multiplying first and second stage input signals.